ABHISHEK SHARMA

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abhishek-sharma-19april1965 | Abhishek-Sharma182005 | My Portfolio |

Agra, Uttar Pradesh - 282007, India

OBJECTIVE

Ambitious Pre-final year student with a strong foundation in VLSI design, Electronics Circuit and Embedded System , driven by a mission to excel in the semiconductor/VLSI industry. Committed to contributing to an organization that values innovation and engineering excellence by delivering efficient and advanced digital solutions.

EXPERIENCE

- **Semiconductor Laboratory (MeiY, Government of India)** *June 2024 - July 2024*
  Advanced VLSI Design Intern Chandigarh, India
  - Conducted research in VLSI technology, focusing on semiconductor manufacturing processes and designed LNA for Navigation Application.
- **CSIR-CEERI** *January 2024*
  Engineering Trainee Pilani, India
  - Completed the Semiconductor High-Impact Learning Program (SHILP), mastering key manufacturing processes.
- **FlexiGate Technologies** *March 2024 - September 2024*
  Hardware Design Intern New Delhi, India
  - Designed PCBs and conducted testing to improve performance and reliability.
- **Technovation Club, Techtronica Society** *September 2023 - Present*
  Vice President [GLA University]
  - Led the Technovation Club to promote technical skill development through workshops, hackathons, and networking events in technology and VLSI.

PROJECTS

- **AI-Based Traffic Management System (Smart India Hackathon 2024)**
  Tools: FPGA (PYNQ-z2) , Xilinx Vivado , VS Code . Python [ ]
  - Developed an FPGA-based intelligent traffic management system to optimize flow and reduce congestion.
  - Implemented real-time algorithms and created a user interface for monitoring traffic patterns.
- **64 bit Single Cycle RISC V Processor**
  Tools: Vivado and EDA Playground [ ]
  - Developed an 64 bit single cycle RISC V Processor
- **Phase Locked Loop**
  Tools: cadence Virtuoso and spectra [ ]
  - Designed PLL for Low Frequency Applications specially for Microprocessors.
  - I have also made it layout in GPDK 90nm technology node ensuring DRC and LVS.
- **PragatiX: Wearable Tech and Green Solutions for Empowering Delivery Workforce**
  Tools: Github, GitLab , Embedded Systems ,Web Development [ ]
  - Designed products and software to empower delivery workforce under Smart India Hackathon 2024

EDUCATION

- **B.Tech in Electronics and Communication Engineering (Specialization in VLSI)** *2023-2026*
  GLA University , Mathura Mathura,Uttar Pradesh, India
  - CPI: 8.6
- **Diploma in Electronics Engineering (Modern Consumer)** *2020 - 2023*
  RBS Polytechnic Agra, Uttar Pradesh, India
  - Grade: 78.5% or CGPA: 8.2
- **High School** *2019 - 2020*
  R.B Public School Agra, Uttar Pradesh, India
  - Grade: 85%

Patents and Publications

J=Journal, P=Patent

[J.1] Abhishek Sharma, Dheeraj Kalra, Manish Kumar , Rajiv Bhatia. (2024). **Design of CMOS Low Noise Amplifier With Inductive Degeneration for Navigation Application**. *Journal of Electrical Engineering*, Vol. 75, Issue 6, pp. 458-466. DOI:10.2478/jee-2024-0054

[P.1] Abhishek Sharma, Gati Goyal , Abhay Chaturvedi , Pattima Bachan (2024). **AI Based Traffic Management System Using FPGA Technology**. Patent Office: New Delhi,India, Patent No. 45/2024 Registration Date: 26/10/2024, Publication Date: 08/11/2024 Grant Date: Pending.

[P.2] Abhishek Sharma, Abhay Chaturvedi, Pattima Bachan (2024). **GSM Based Vehicle Accident Alert Smart System** . Patent Office: New Delhi,India, Patent No. 48/2024 Registration Date: Sept 2024, Publication Date: 29/11/2024, Grant Date: Pending.

Skills

- **Programming Languages:** Python, C, C++, System Verilog, Verilog ,CSS ,HTML
- **VLSI Tools & Technologies:** Cadence Virtuoso, EasyEDA, Xilinx Vivado, VS Code ,MATLAB , ADS
- **Specialized Area:** Digital Design, FPGA Development, RTL Design, VLSI Design
- **Research Skills:** Literature Review, Experimental Design, Data Analysis, Technical Writing, Presentation Skills, Problem Solving

Honors and Awards

- **SIH 2024 Winner and Team Leader**
  Smart India Hackathon 2024, Ministry of Education, Govt. of India
  - Won first place in a national-level hackathon with innovative solutions for urban resource management and logistics.
  - Led the development of an IoT-based prototype to enhance urban infrastructure.
- **Co-Instructor** *October 2024*
  Techtronica Society, GLA University
  - Received a memento from the Head of Department for co-instructing the "Smart Solutions with Arduino and Raspberry Pi" workshop and guiding students through projects from LED blinking to advanced automation systems.

Leadership Experience

- **Advanced 108 RTL Projects Team Leader** Aug 2024 - Dec 2024
  Independent Research, GLA University
  - Led 108 RTL projects, showcasing expertise in digital design and synthesis.
  - Optimized and verified complex RTL modules for efficient, scalable circuits.
  - Mentored peers and juniors in RTL design, improving project quality.

Volunteer Experience

- **Social Entrepreneur Intern** *February 2022*
  Hamari Pahchan, New Delhi, India [🌐]
  - Conducted research and led impactful social media campaigns to raise awareness on social issues, reaching a broader audience.
- **3rd International IEEE CCIS Conference** *February 2022*
  GLA University , MAthura , Uttar Pradesh [🌐]
  - Conducted research and led impactful social media campaigns to raise awareness on social issues, reaching a broader audience.

Certifications

- **Cadence Design Systems:** RTL-to-GDSII Flow, Semiconductor 101, Cadence Student Ambassador *2024*
- **NPTEL:** C-Based VLSI Design *October 2024*
- **Cadence Design Systems:** Digital Physical Design Domain, Front End Digital Design and Verification Language *2024-2025*

Additional Information

Languages: Hindi (Native), English (Fluent)
Interests: DIY Projects, Nature Hiking, Embedded Systems, VLSI, AI in Semiconductors, Sci-Fi Reading.

References

1. **Dr. V.K Tomar**, Professor, ECE, GLA University
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2. **Dr. Manish Kumar**, Associate Professor, ECE, GLA University
   manish.kumar@gla.ac.in | +91 97192-32004 | *Mentor*